

STF40NF06

General features

Туре	V _{DSS}	R _{DS(on)}	I _D
STF40NF06	60V	<0.028Ω	23A

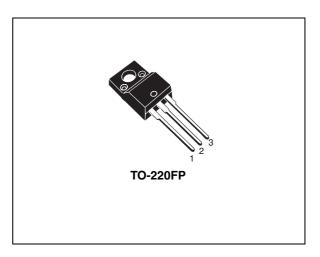
- Exceptional dv/dt capability
- Low gate charge at 100°C
- Application oriented characterization
- 100% avalanche tested

Description

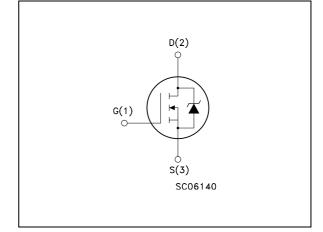
This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Applications

Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STF40NF06	F40NF06	TO-220FP	Tube

September	2006
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Electrical ratings

Table 1. Absolute maximum rating

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage ($V_{GS} = 0$)	60	V
V _{GS}	Gate-source voltage	± 20	V
۱ _D	Drain current (continuous) at $T_C = 25^{\circ}C$	23	А
۱ _D	Drain current (continuous) at $T_C=100^{\circ}C$	16	А
I _{DM} ⁽¹⁾	Drain current (pulsed)	92	А
P _{TOT}	Total dissipation at $T_C = 25^{\circ}C$	30	W
	Derating Factor	0.2	W/°C
dv/dt ⁽²⁾	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	250	mj
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s; Tc= 25°C)	2500	v
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 40A$, di/dt $\leq 300A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $Tj \leq T_{JMAX}$

3. Starting $T_j = 25^{\circ}C$, $I_D = 20A$, $V_{DD} = 30V$

R _{thj-case}	Thermal resistance junction-case Max	5.0	°C/W
Τ _Ι	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_{D} = 250 \ \mu A, \ V_{GS} = 0$	60			V
I _{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	V _{DS} = Max rating, V _{DS} = Max rating @125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20V$			± 100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2		4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 11.5A		0.024	0.028	Ω

Table 3. On/off states

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} (1)	Forward transconductance	V _{DS} = 30V, I _D = 11.5A		12		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} =25V, f=1 MHz, V _{GS} =0		920 225 80		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} =48V, I _D = 10A V _{GS} =10V		32 6.5 15	43	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r	Turn-on Delay Time Rise Time	$V_{DD} = 30V, I_D = 20A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 13)		27 11		ns ns
t _{d(off)} t _f	Turn-off-delay time Fall time	$V_{DD} = 30V, I_D = 20A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 13)		27 11		ns ns



Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I _{SD}	Source-drain current				23	А
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				92	А
$V_{SD}^{(2)}$	Forward on voltage	I _{SD} =23A, V _{GS} =0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} =40A, di/dt = 100A/μs, V _{DD} =10V, Tj=150°C (see Figure 15)		63 150 4.8		ns nC A

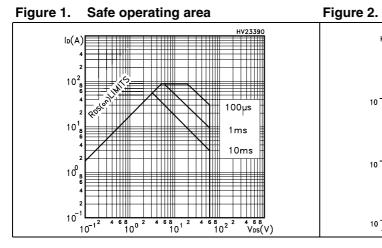
 Table 6.
 Source drain diode

1. Pulse width limited by safe operating area

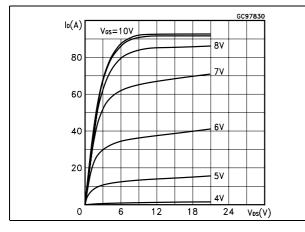
2. Pulsed: pulse duration=300µs, duty cycle 1.5%



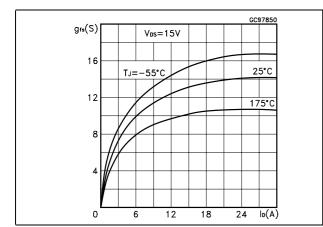
2.1 Electrical characteristics (curves)

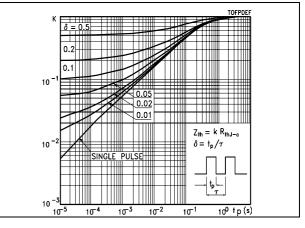












Thermal impedance

Figure 4. Transfer characteristics

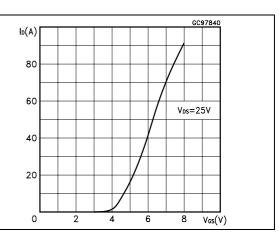
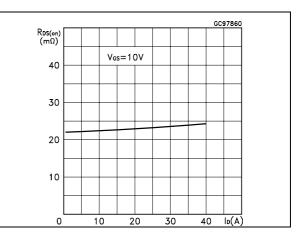


Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

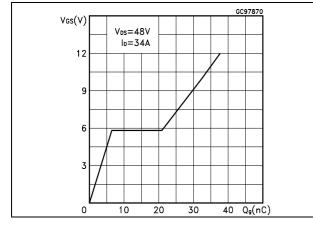


Figure 9. Normalized gate threshold voltage vs temperature

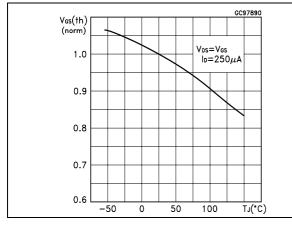
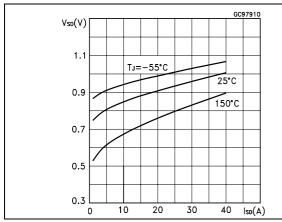


Figure 11. Source-drain diode forward characteristics



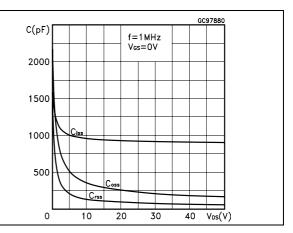


Figure 10. Normalized on resistance vs temperature

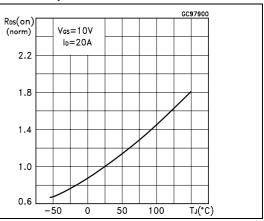
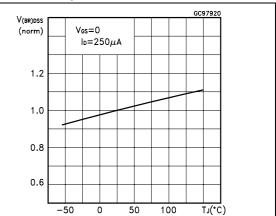


Figure 12. Normalized breakdown voltage vs temperature



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3 **Test circuit**

Figure 13. Switching times test circuit for resistive load

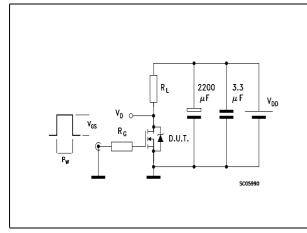
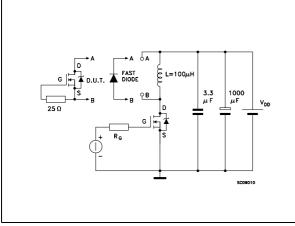


Figure 15. Test circuit for inductive load switching and diode recovery times





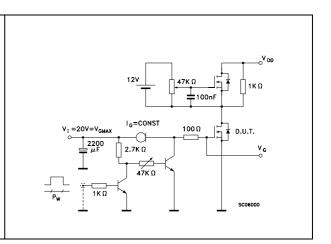


Figure 16. Unclamped Inductive load test circuit

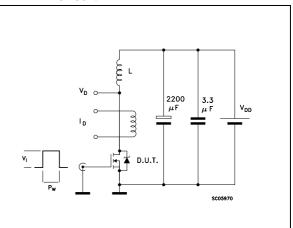


Figure 18. Switching time waveform

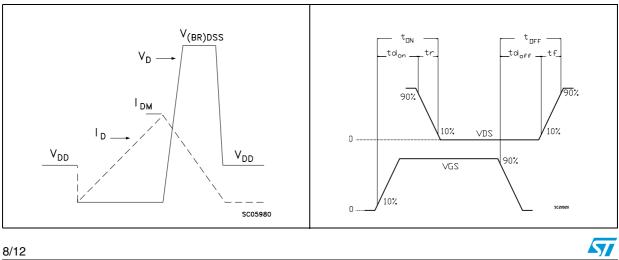


Figure 14. Gate charge test circuit

4 Package mechanical data

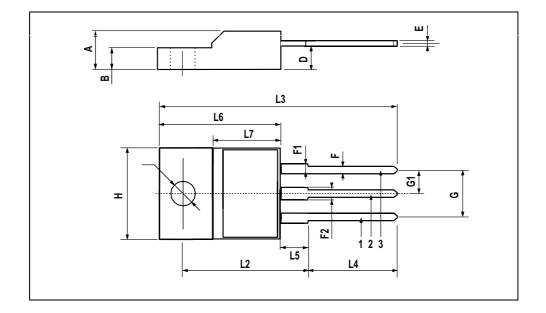
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



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DIM.	mm.			inch		
	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX.
А	4.4		4.6	0.173		0.181
В	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
Н	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126

TO-220FP MECHANICAL DATA



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5 Revision history

Table 7.	Revision	history
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Date	Revision	Changes
12-Nov-2004	1	First release
27-May-2005	2	Final datasheet
04-Sep-2006	3	New template, no content change



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